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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,610	03/06/2002	Yutaka Mimino	020124	4961

23850 7590 01/15/2003

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,610	MIMINO ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamasaki et al. U.S. Patent 5,973,554.

Yamasaki et al. disclose in Figures 2A and 2B and respective portions of the specification a multilevel wiring structure for semiconductor devices wherein two levels of metalization is used for connection to a gate of a transistor which results in less power supply noise (Abstract).

Specifically, Yamasaki et al. disclose a multilayer wiring structure for semiconductor devices, comprising:

a semiconductor substrate 71;

at least one active region 73 supplied with an electric power from a power-supply potential VCC; and

a plurality of power-supply lines 4 and 5 for supplying with the electric power to said active region therethrough, said power-supply lines disposed at different layers of the multilayer wiring structure on said semiconductor substrate and being connected in parallel to each other.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Lu et al. U.S. Patent 6,100,573.

Lu et al. disclose in Figures 3A-3D, particularly Figure 3A, and respective portions of the specification a multilevel wiring structure for semiconductor devices having improved adhesion and reduced stress wherein multiple levels of metalization are connected in parallel. Specifically, Lu et al. disclose a multilayer wiring structure for semiconductor devices, comprising:

a semiconductor substrate 300;

at least one active region (not shown) supplied with an electric power from a power-supply potential (column 3, lines 60-67, "The denotation 330 represents a position to which the external signal is inputted or outputted, such as a power signal, a ground signal, or an input/output signal"); and

a plurality of power-supply lines 304, 306, and 308 for supplying with the electric power to said active region therethrough, said power-supply lines disposed at different layers of the multilayer wiring structure on said semiconductor substrate and being connected in parallel to each other.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Correale, Jr. U.S. Patent 5,789,807.

Correale discloses in Figures 5A, 5B, and respective portions of the specification a multilevel wiring structure for semiconductor devices having improved decoupling capacitance for power conductors in parallel metal layers (Abstract). Specifically, Correale discloses a multilayer wiring structure for semiconductor devices, comprising:

a semiconductor substrate (not shown);

at least one active region (not shown) supplied with an electric power from a power-supply potential Vdd; and

a plurality of power-supply lines Vdd for supplying with the electric power to said active region therethrough, said power-supply lines disposed at different layers of the multilayer wiring structure on said semiconductor substrate and being connected in parallel to each other.

5. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Mimoto et al. U.S. Patent 6,326,693.

Mimoto et al. disclose in Figures 5-15, and respective portions of the specification a multilevel wiring structure around core circuits for decreasing interconnection area, wherein the multilevel wiring structure comprises all limitations as claimed.

Referring to claim 1, Mimoto et al. disclose in Figure 5 a multilayer wiring structure for semiconductor devices, comprising:

a semiconductor substrate (not shown);

at least one active region (not shown) supplied with an electric power from a power-supply potential Vdd; and

a plurality of power-supply lines 4a-4d, for supplying with the electric power to said active region therethrough, said power-supply lines disposed at different layers of the multilayer wiring structure on said semiconductor substrate and being connected in parallel to each other (note that dashed lines are in one level and solid lines are in another level).

Still referring to claim 1, Mimoto et al. disclose in Figure 14 a multilayer wiring structure for semiconductor devices, comprising:

a semiconductor substrate (not shown);

at least one active region (not shown) supplied with an electric power from a power-supply potential; and

a plurality of power-supply lines 41, 42, 33, 34 ("reinforcing lines") for supplying with the electric power to said active region therethrough, said power-supply lines disposed at different layers of the multilayer wiring structure on said semiconductor substrate and being connected in parallel to each other.

Regarding claim 2, Mimoto et al. further discloses a common power-supply line 5b which is connected to the power-supply lines and which has a current-carrying capacity larger than that of each of the power-supply lines 41, 42, 33, 34, is provided between said power-supply potential and said active region.

Although not explicitly disclosed, common power-supply line 5b has a current-carrying capacity larger than that of each of the power-supply lines 41 and 42 the combination of which supplies power to the common power-supply line 5b.

Referring to claim 4, Figure 14 further depicts that the common power-supply line 5b is provided between said active region and said power-supply lines.

Regarding claim 5, Mimoto et al. further discloses that the common power-supply line 5b is provided between said power-supply potential and said active region, with both ends thereof connecting to the power-supply lines 41, 42, and 33, 34.

With respect to claim 6, although not shown, it is extremely unlikely that the LOGIC portion has only one element. Therefore, it is safe to conclude that the power-supply lines connect in parallel to the active regions.

Regarding claims 3 and 7, although Mimoto et al. do not disclose a connection pad, the disclosed structure must include connection pads to function.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Correale.

Referring to claim 2 and Figure 5A of the Correale's reference, common power-supply line 503 ("stitches") appears to have a width larger than that of either power-supply line Vdd in the M1 layer or the power-supply line Vdd in the M3 layer. Specifically, Figure 5A depicts a multilayer wiring structure for semiconductor devices having all limitations as detailed above for claim 1, wherein a common power-supply line 503 which is connected to the power-supply lines and which has a current-carrying capacity larger than that of each of the power-supply lines is provided between said power-supply potential and said active region.

Referring to claims 3-7, the structure depicted in Figure 5A and other portions of the specification comprises all limitations as similarly detailed above in paragraph 5.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent 6,489,671 to Aoki et al. discloses a three-dimensional interconnection line structure for high-speed operation in a MMIC.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (703) 305-0086. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tu-Tu Ho
January 08, 2003

HOAI HO
PRIMARY EXAMINER